PATENT #11 D
Turner B
6/23/97

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Charles H. Moore et al.

Serial No. 08/484,935

Filed: June 7, 1995

For: HIGH PERFORMANCE MICROPROCESSOR USING INSTRUCTION GROUPS

Examiner: D. Eng

Group Art Unit: 2315

Palo Alto, CA

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to the Assistant Commissioner for Patents Washington, D.C. 20231, on June 12, 1997.

Date: 6-12-97 By: Patricia K. Parry
Patricia K. Parry

6/26/97

AMENDMENT

Commissioner of Patents
and Trademarks
Washington, D.C. 20231

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Sir:

In response to the Office Action dated December 12, 1996, please amend the above application as follows:

In the Title:

After "HIGH PERFORMANCE MICROPROCESSOR USING", delete "INSTRUCTION GROUPS" and substitute --INSTRUCTIONS THAT OPERATE WITHIN INSTRUCTION GROUPS--.

In the Specification:

At the beginning of the specification, delete the text of the present Cross Reference to Related Applications, and substitute: --This application is a division of U.S. Application Serial No. 07/389,334, filed Aug. 3, 1989, now U.S. Patent 5,440,749.--.

D1

Page 3, line 7, before "memory", and line 8, after "and the", in each case, delete "dynamic random access".

Page 3, lines 9-13, delete "There is a multiplexing means on the bus between the central processing unit and the dynamic random access memory. The

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